An Analog Structural Synthesis Approach using
Signal Interaction Diagrams

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Abstract. This paper presents a methodology for the structural synthesis of analog circuits. Starting from a directed signal parameter flow representing the information processing, the synthesis is done by a formal, knowledge based approach. This approach uses a qualitatively characterized structural design representation, the signal interaction diagram. The description of an analog implementation of a switch in a particular application serves as example for the specific design flow.

I. Introduction

The interfaces of electronic information processing ICs are mostly composed of analog modules for performing data and signal conditioning. Even for analog system components, great efforts have been made to enable high-level design methodologies.

In the late 1980’s, the structural synthesis of analog blocks was based on architectural selection [1][2]. In connection with hierarchical decomposition, design automation tools became more flexible in the early 1990’s [3]–[6]. Besides simulation based methods [7][6], analytical [2] and formal [8][9] approaches were established for sizing, specification refinement, and the evaluation of specific topologies. Then, formal techniques were introduced to the process of structural synthesis [10].

Formal techniques enable design approaches starting from algorithmic, or data flow specifications [11]. From the abstraction point of view, the data flow gives the basis to both digital signal processing and analog circuit implementations. Thus, the focus is put on data processing analog components, such as sensoric front ends, and on communication systems. But there is no general approach to overstep the gap between the structures of high-level and electrical design representations.

In [12], a design strategy is outlined, which is based on a multi-phase design flow, separating the design of the data flow and the design of the electrical signal flow. All steps for designing the data flow belong to the analog functional synthesis and all steps for designing the energy flow belong to the electrical synthesis.

Here, the approach for the synthesis of the electrical device structure is introduced.

II. The Design Flow

A multi-phase design flow enables us to split the overall synthesis process into two phases: An analog functional synthesis that is oriented towards information processing, and an electrical synthesis oriented towards analog circuit operation.

In the function-driven design phases, structural selection and decomposition is done on the basis of the system’s or circuit’s function and on the basis of classified properties of the data or the signals, corresponding to the level of abstraction. Thereby, only main principles are to be taken into account; more complex structures are established by means of formal methods.
The sizing-oriented design phases are starting from symbolic relations, expressing functional relations between the elements. According to the level of abstraction, data or signal parameter values are considered, which are derived from the design specifications. Additionally, sizing-dependent structural transformations are applied. On the one hand, these transformations take the dependency of structural selection from the specific sizing into account and, on the other hand, these transformations drastically reduce the number of alternatives that have to be taken into consideration in each structural selection step.

III. The Signal Interaction Diagram

A. Electrical Domain Design Representations

In the electrical domain, the design is given by a structure of electronic devices, and, at a higher level of hierarchy, by blocks of devices.

The behavior of the design is derived from the device primitives behavioral models by means of the nodal analysis, for example. Beside application independent electrical models, a higher level of abstraction is enabled by using functional models. Due to the facts that these functional models are expressed by node voltages and branch currents, this level of abstraction belongs to the electrical domain.

![Resonant circuit example]

Fig. 1 Resonant circuit example: a) device structure, b) signal flow, c) scattering flow

The electrical domain behavioral descriptions may be represented by means of directed signal flow graphs, the so called Mason graphs [13][14]. Functional models provide simplified graphs by focusing on special aspects. For example, the usage of AC models eliminates the operating point feeding. The two-way connected, directed graph expresses the strong interaction between the devices of analog circuits. For example, Fig. 1 b) shows the signal flow of the resonant circuit in Fig. 1 a).

A scattering parameter based behavioral description gives the directed power flow in the electric circuit [15]. The wave parameters \(a\) and \(b\) represent the in- and outgoing voltage waves \(V^+\) and \(V^-\) according to

\[
a_n = \frac{V^+_n}{\sqrt{R_n}} \quad \text{and} \quad b_n = \frac{V^-_n}{\sqrt{R_n}}
\]

with \(R_n\) denoting the characteristic impedance. Fig. 1 c) shows the scattering flow of the resonant circuit. The reflection factors are known to be

\[
\varphi = \frac{R - R_n}{R + R_n}.
\]

On this basis, the electrical signal may be decomposed in orthogonal components, represented by power channels. The scattering parameter based model is represented by a Mason graph, too.

B. Structural Interpretation

In order to build up a circuit structure, a structural design representation is needed. By the use of this design representation, the connectability of two elements representing device principles has to
be decided on a qualitative basis. Furthermore, several design alternatives may be considered without drastically changing the design structure even if these alternatives lead to different circuit topologies. The signal interaction diagram provides a structural design representation useful for this synthesis task, and it is derived as follows:

The device principles can be modeled by scattering parameter based signal flow graphs. Every orthogonal signal component, relevant for the device principle’s model from the functional point of view, is assigned to a signal interaction channel, as it is called here. In this way, physical signals are disassembled into signal components. The decomposition of electrical signals into orthogonal power flow channels gives freedom to the subsequent synthesis phase, since the allocation of the power flow channels to electrical nodes is kept open. The signal interaction channel based electrical model is related to the information flow by formal transformation according to the relations between the signal parameters carrying information and the electrical signals.

![Fig. 2 Interconnection model simplification: a) circuit model, b) open circuit example](https://example.com/fig2)

In order to build up a circuit structure by connecting device principles, qualitative characterizations of the signal interaction channels are required.

First, the signal flow graph is simplified with respect to idealized impedance relations. Up to now, there is no quantitative parameter for the impedance relation available, since the sizing depends on the still unknown circuit structure. Three cases have to be considered: The error free propagation of a voltage signal from a source to a load port requires an open circuit impedance relation. This corresponds to a source reflection factor $\rho_s = -1$ and a load reflection factor $\rho_l = +1$. Assuming neglectable transmission line effects, the signal flow graph is simplified by loop elimination as shown in Fig. 2 b). In the same way, for the error free propagation of a current signal a short circuit impedance relation is needed, and in some cases, the propagation of a power signal is required.

![Fig. 3 a) Simplified scattering signal flow of a ohmic admittance, b) Reduced scattering signal flow, c) Primary and parasitic signal components in the reduced scattering signal flow](https://example.com/fig3)

From the functional point of view, an ohmic admittance may be used as a voltage-current converter with an open circuit relation at its input, and a short circuit relation at its output channel. Fig. 3 a) shows the simplified, functional scattering signal flow graph.
Assuming idealized impedance relations, each pair of wave parameters $a$ and $b$ may be represented by one graph node as shown in Fig. 3b). Here, the nodes are characterized by the reflection factor between $a$ and $b$.

For realistic synthesis results, parasitic signal components are associated to the signal interaction channels. A signal interaction channel consists of a primary signal component according to the device principle function, and several signal components expressing functional errors. By connecting device principles according to equivalent characterizations of the primary signal components, a functional error may arise from a path of parasitic signal components with equivalent characterizations and directions. In the example of the ohmic admittance, there are two parasitic signal components describing the deviation caused by the input current, and by the output voltage, respectively. In Fig. 3c), the primary components are marked by solid dots in the reduced scattering signal flow.

The signal interaction diagram represents the structure of electrical device principles by characterized, directed signal interaction channels. According to the idealized impedance relations, the connectability of device principles is described by an ideal open (+), short (−) or matched (0) impedance relation.

The line mode describes the physical nodes associated with the signal interaction channel to be driven in a balanced (double flag) or in an unbalanced mode (single flag).

The signal mode describes the frequency range (operation point $op$, quasi-static $qst$, baseband $bb$, sideband $sb$, ...), or the time slot the signal belongs to. Parallel to the information oriented signal flow, the bias feedings are structured according to the operation point signal mode.

Fig. 4 shows the signal interaction diagram of a simple voltage divider, composed of the device principles MOS-channel admittance and MOS-channel impedance. According to the parasitic signal path between the device principles, the MOS-channel admittance and the MOS-channel impedance must not be connected without any additional effort. Thus, the electrical synthesis concludes element detections and manipulations, guided by the characterizations of the signal interaction model.

**IV. The Electrical Conditioning Synthesis**

**A. Information Domain Model**

From the structure point of view, the information domain is characterized by functional blocks representing principles of implementation. A principle of implementation is designated by qualitative characterizations of the data regarding the signal parameter that carry information, the value domain, and the characteristics of the events representing data validity in the time domain. Whereas this level of abstraction enables known high-level design methodologies, the principles of implementation consider
the capabilities of analog systems. Fig. 5 shows the functional blocks of a two-value reference level switch, derived by the analog functional synthesis.

![Fig. 5 Switch decomposition](image)

The quantitative, e. g. behavioral, model on this level of abstraction is called signal parameter flow. Here, parameter sources and drains are assigned to the inputs and outputs of each functional block, quantitatively representing the properties of the corresponding signal parameters, such as the modulation ranges of the information carriers, their tolerance bounds by error limits $\Delta$, or by variance $\sigma$, their bandwidth, and, if necessary, the sampling rate. Due to the top-down design strategy, the electrical synthesis starts from this model.

**B. The Structural Synthesis Step**

The structural synthesis step is done by identifying the device principles from the signal parameter flow by a tolerant pattern recognition approach, and by applying transformation rules. The device level structure is build up by connecting the device principle primitives according to their interface characteristics.

In the first synthesis step of the switch example, the device principles *MOS-channel admittance* and *modulated MOS-channel impedance* are selected from the design knowledge database, since their functional level behavioral models match to the signal parameter flow. This information to electrical domain mapping is done on the basis of known model relations between the device level structural elements, the device principles shown in the signal interaction diagram, and the functional level behavioral model, represented by signal parameter flow graphs stored in the design database. Within this mapping, sizing relations for the device principles parameters are derived from the signal parameter flow:

$$Y_{DS} = \frac{1}{b}, \quad R_{DS1} = a_1, \quad R_{DS2} = a_2.$$

As it is shown in Fig. 6 a), the MOS-channel admittance and the modulated MOS-channel impedances must not be connected, since these connections lead to parasitic interaction paths.

The parasitic interaction paths may be conditioned by either inserting insulating device principles or by applying transformations. In both cases, the design decisions can be represented by device or circuit principles in the signal interaction diagram, and are the result of a selection process. This structural selection process is guided by the priority of the design alternatives, given by the inverse of the number of elements plus the number of parameters to be detected by a sizing step.
Here, the parasitic interaction loop is eliminated by a sizing rule representing a device parameter splitting transformation, giving a corrected admittance parameter

$$Y'_{DS} = \frac{Y_{DS}}{1 - R_{DS1}Y_{DS} - R_{DS2}Y_{DS}}.$$  

According to Fig. 6 b), this sizing rule is represented by a conditional circuit principle to be applied to the MOS-channel admittance, and thus eliminating the parasitic interaction loop.

Taking into account the functional level parameter values of $b$, $a_1$ and $a_2$ performing the relation
\[ b = a_1 + a_2 \] in the data sizing step, the sizing rule gives

\[ y_{DS}' \to \infty. \]

As a result, this condition stimulates the admittance to be replaced by a series connection, since there is no more separate admittance device principle needed. Fig. 6c) shows the resulting structure of device and circuit principles on the device level.

V. Implementation and Results

The use of signal interaction diagrams enables the synthesis of the device level structure, giving the topology of device and circuit principles. According to the design methodology, the structure of electrical devices will be derived by the next design step, the device synthesis.

The signal interaction diagram based approach enables formal descriptions of more abstract and elementary circuit principles. By means of the signal interaction diagram, the connectability of a number of analog device or circuit primitives can be decided in a formal way. Due to the good conformity between data flow and energy flow based design representations, the signal interaction diagram closes the gap between the high-level and the electrical domain.

Compared with traditional approaches, the electrical domain elements are of less complexity, since only functional aspects are to be considered in the electrical domain. Interface adaptions, signal conditioning, and operating point feedings are taken into account by its own device principles.

Up to now, the approach is demonstrated by two applications. The analog implementation of a modulo operator uses node voltages and branch currents to represent information. The switch example, demonstrated in this paper, is part of this modulo operator application. A quadrature demodulator sensor front end additionally requires phase and frequency parameters in the information domain. The main focus of this work is the definition of the design steps for implementing the design methodology.

The success of this structural synthesis approach is based on the formal description of the design primitives according to the levels of abstraction. Here, a clear understanding of the insights of the device and circuit principles and their functions is needed. In order to verify the universal synthesis approach, more properly modeled design primitives are needed.

The approach introduced here is implemented by Mathematica packages, providing an experimental system. However, Mathematica is unable to manage huge amounts of design data primitives, representing the design knowledge. Here, parts of the design data management, such as the design graph database and pattern recognition engine, as well as the design graph visualization are implemented by external C- and Java-routines, and are linked to Mathematica via the MathLink and J/Link interfaces.

References


